CLAIMS

1. A programmable logic device, comprising an active logic section and a configuration memory, wherein the active logic section and the configuration memory have separate power supply connections.

2. A programmable logic device as claimed in claim 1, wherein the active logic section comprises a gate array.

3. A programmable logic device as claimed in claim 2, wherein the active logic section further comprises an embedded logic device, and the gate array and the embedded logic device have separate power supply connections.

4. A programmable logic device as claimed in claim 3, wherein the logic device comprises an embedded processor.

5. A programmable logic device as claimed in claim 1, further comprising a programmable input/output section, wherein the programmable input/output section has a further separate power supply connection.

6. A programmable logic device as claimed in claim 1, wherein the configuration memory has power supply connections to power supplies at two different voltages.

7. A programmable logic device integrated circuit, having a plurality of pins for connection to respective other devices, the programmable logic device integrated circuit comprising an active logic section and a configuration memory, wherein the active logic section is connected to at least a first pair of said pins to receive power therefrom, and the configuration memory is connected to a second pair of said pins different from the first to receive power therefrom.

8. A programmable logic device integrated circuit as claimed in claim 7, wherein the active logic section comprises a gate array.

9. A programmable logic device integrated circuit as claimed in claim 8, wherein the active logic section further comprises an embedded logic device, and the gate array is connected to said first pair of said pins to receive power therefrom, and the embedded

logic device is connected to a third pair of said pins different from the first to receive power therefrom.

10. A programmable logic device integrated circuit as claimed in claim 9, wherein the embedded logic device further comprises an embedded processor.

11. A programmable logic device integrated circuit as claimed in claim 7, further comprising a programmable input/output section, wherein the programmable input/output section is connected to a fourth pair of said pins different from the first and second to receive power therefrom.

12. In a programmable logic device, comprising an active logic section and a configuration memory, a method comprising operating the device in a first mode of operation, in which power is supplied to the configuration memory and power is disconnected from the active logic section.

13. A method as claimed in claim 12, wherein the active logic section comprises a gate array and an embedded logic device, the method further comprising operating the device in a second mode of operation, in which power is supplied to the gate array of the active logic section and power is disconnected from the embedded logic device.

14. A method as claimed in claim 12, wherein the programmable logic device further comprises a programmable input/output section, wherein, in the first mode of operation, power is supplied to the programmable input/output section.

15. A method as claimed in claim 12, the method further comprising operating the device in a normal mode of operation, in which power is supplied to the configuration memory and to the active logic section.

16. A method as claimed in claim 15, the method further comprising supplying a first voltage to the configuration memory in said normal mode of operation and supplying a second voltage, lower than said first voltage, to the configuration memory in said first mode of operation.

17. A method as claimed in claim 12, further comprising:

before entering said first mode of operation, storing data from registers of said active logic section in a memory device separate from said programmable logic device; and

after completing said first mode of operation retrieving said data, stored in said separate memory device, into the registers of said active logic section.

18. An electronic device comprising a power supply and a programmable logic device integrated circuit, wherein the power supply comprises a plurality of power supply rails, and the programmable logic device integrated circuit comprises an active logic section and a configuration memory, wherein the active logic section is connected to a first pair of said power supply rails through a first pair of said pins on said integrated circuit to receive power therefrom, and the configuration memory is connected to a second pair of said power supply rails through a second pair of said pins different from the first to receive power therefrom.

19. An electronic device as claimed in claim 18, wherein the power supply comprises a plurality of power supply rails at different respective voltages, and the active logic section and the configuration memory are connected to power supply rails at different respective voltages.

20. An electronic device as claimed in claim 18, wherein the active logic section of the programmable logic device integrated circuit comprises a gate array.

21. An electronic device as claimed in claim 20, wherein the active logic section of the programmable logic device integrated circuit further comprises an embedded logic device, and the gate array is connected to said first pair of said pins on said integrated circuit to receive power therefrom, and the embedded logic device is connected to a third pair of said pins on said integrated circuit different from the first pair to receive power therefrom.

22. An electronic device as claimed in claim 18, wherein the programmable logic device integrated circuit further comprises a programmable input/output section, and wherein the programmable input/output section is connected to a fourth pair of said pins on said integrated circuit different from the first and second pairs to receive power therefrom.

23. An electronic device as claimed in claim 19, wherein said configuration memory is connected to power supply rails at two different voltages.

24. An electronic device as claimed in claim 23, wherein, when the active logic section is connected to said first pair of said power supply rails through said first pair of said pins on said integrated circuit to receive power therefrom, the configuration memory is connected to said second pair of said power supply rails through said second pair of said pins different from the first to receive power therefrom, and, when the active logic section is disconnected from said first pair of said power supply rails, the configuration memory is connected to a third pair of said power supply rails through a fifth pair of said pins to receive power therefrom at a reduced voltage.

25. An electronic device as claimed in claim 24, further comprising a memory device, wherein, when said active logic section is to be disconnected from said first pair of said power supply rails, data stored in registers of said active logic section is transferred to said memory device.